

SL3S1004_1014

UCODE 7xm and UCODE 7xm+

Rev. 3.2 — 27 July 2016
325032

Product data sheet
COMPANY PUBLIC

1. General description

The UCODE 7xm series is the latest generation of NXP's memory UHF tag ICs. With the leading-edge read range UCODE 7xm is well suited for applications which require high read range and also demanding an extended user memory to store data specific to customer or products. UCODE 7xm offers an user memory of 1-kbit, whereas UCODE 7xm+ supports 2-kbit user memory and a 384-bit digital signature.

Both products incorporate features known from UCODE 7 like pre-serialization, tag power indicator as well as the product status flag.

There are numbers of applications where the combination of high read range and user memory is needed, such as:

- Inventory and supply chain management
- Process optimization (e.g in the automotive industry)
- Brand protection/authentication (e.g. expensive wines or branded luxury fashion items)
- Automatic vehicle ID where no cryptography is required
- Asset tracking (e.g. for high value assets)

2. Features and benefits

2.1 Key features

- Read sensitivity –19 dBm
- Write sensitivity –12 dBm
- Encoding speed: 32 bits per 1.5 milliseconds
- Up to 2-kbit user memory
- Digital signature
- Standard functionality
 - ◆ Untraceable feature
 - ◆ Tag Power Indicator
 - ◆ Pre-serialization for 96-bit EPC
 - ◆ Integrated Product Status Flag (PSF)
 - ◆ Parallel encoding mode
- According to EPCglobal v1.2.0
- Compatible with single-slit antenna



2.1.1 Memory

- Up to 448-bit of EPC memory
- Supports Pre-serialization for 96-bit EPC
- 96-bit Tag Identifier (TID) factory locked
- 48-bit unique serial number factory-encoded into TID
- 1-kbit user memory for UCODE 7xm
- 2-kbit user memory for UCODE 7xm+
- 384-bit digital signature in UCODE 7xm+
- 32-bit kill password to permanently disable the tag
- 32-bit access password
- Wide operating temperature range: -40 °C up to +85 °C
- Minimum 100.000 write cycle endurance
- Data retention 20 years

2.2 Key benefits

2.2.1 End user benefit

- Extended user memory of up to 2-kbit
- Brand protection feature using digital signature
- Long read/write ranges due to leading edge chip sensitivity
- Reliable operation in dense reader and noisy environments through high interference rejection

2.2.2 Antenna design benefits

- High sensitivity enables smaller and cost efficient antenna designs
- Selected chip impedance enables re-use of antenna designs from UCODE 7

2.2.3 Label/module manufacturer benefit

- Large RF pad-to-pad distance to ease antenna design
- Symmetric RF inputs are less sensitive to process variation
- Single-slit antenna for a more mechanically stable antenna connection
- Pre-serialization of the 96-bit EPC
- Extremely fast encoding of the EPC content

2.3 Supported features

- All mandatory commands of EPCglobal v1.2.0 specification are implemented
- The following optional commands are implemented:
 - ◆ Access
 - ◆ BlockPermalock (block size of 256-bit)
 - ◆ 32-bit BlockWrite
- Implemented custom commands and features:
 - ◆ Untraceable
 - ◆ ReadSignature
 - ◆ Product Status Flag bit: enables the UHF RFID tag to be used as EAS

(Electronic Article Surveillance) tag without the need for a back-end data base.

- ◆ Tag Power Indicator: enables the reader to select only ICs/tags that have enough power to be written to.
- ◆ Parallel encoding: allows for the ability to bring (multiple) tag(s) quickly to the OPEN state and hence allowing single tags to be identified simply, without timing restrictions, or multiple tags to be e.g. written to at the same time, considerably reducing the encoding process

UCODE 7xm can be used in combination with readers compliant with EPCglobal v1.2.0 standard. For access to full UCODE 7xm family functionality firmware upgrade of the reader may be necessary.

3. Applications

3.1 Markets

- Logistics
- Brand protection (luxury branded fashion goods)
- Process automation

3.2 Applications

- Inventory and supply chain management
- Asset tracking
- Process optimization(e.g in the automotive industry)
- Automatic vehicle ID where no cryptography is required
- Brand protection/authentication (e.g. expensive wines or branded luxury fashion items)
- Parking access
- Fleet management
- Loss prevention

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Name	IC type	Description	Version
SL3S1004FUD/BG1	Wafer	UCODE 7xm	Gold bumped die on sawn 8" 120 µm wafer with 7 µm Polyimide spacer;	not applicable
SL3S1014FUD/BG1	Wafer	UCODE 7xm+	Gold bumped die on sawn 8" 120 µm wafer with 7 µm Polyimide spacer;	not applicable

5. Block diagram

The UCODE 7xm/7xm+ consists of three major blocks:

- Analog Interface
- Digital Control
- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader which is then processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital control includes the state machines, processes the protocol and handles communication with the EEPROM, which contains the EPC and the user data.

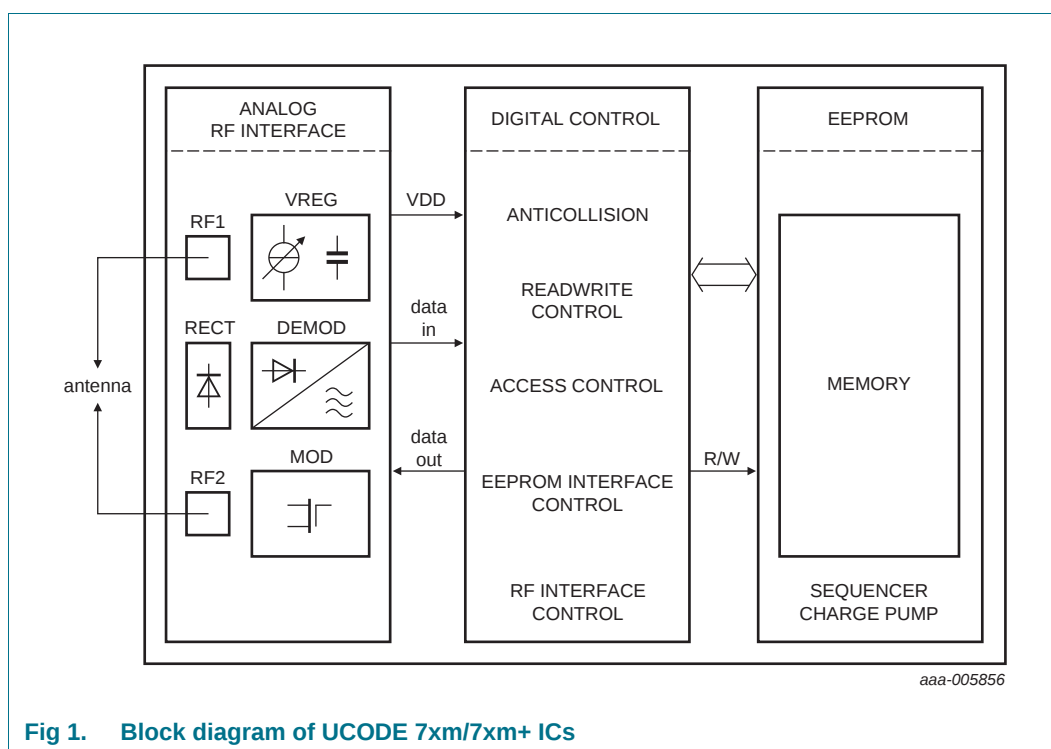
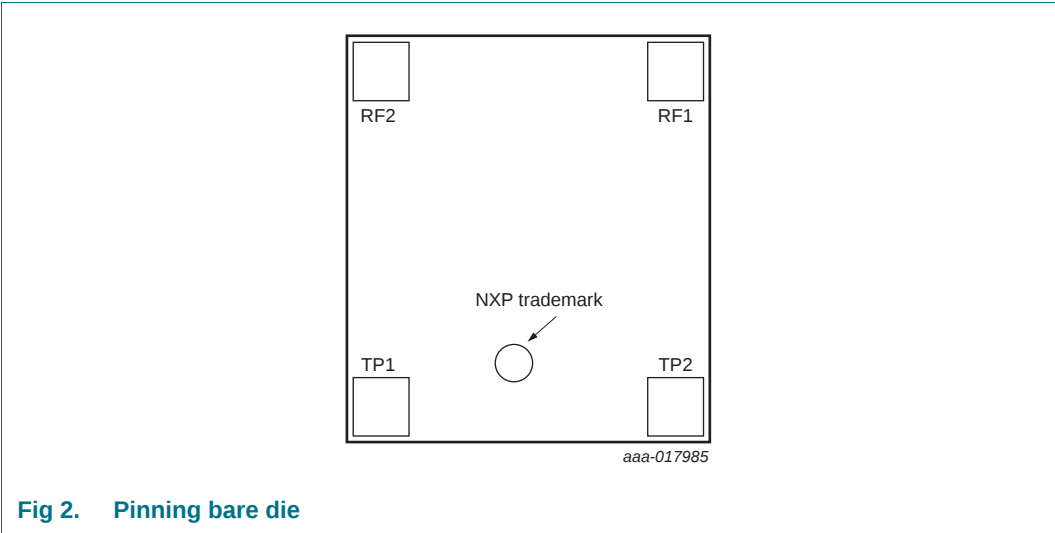


Fig 1. Block diagram of UCODE 7xm/7xm+ ICs

6. Pinning information



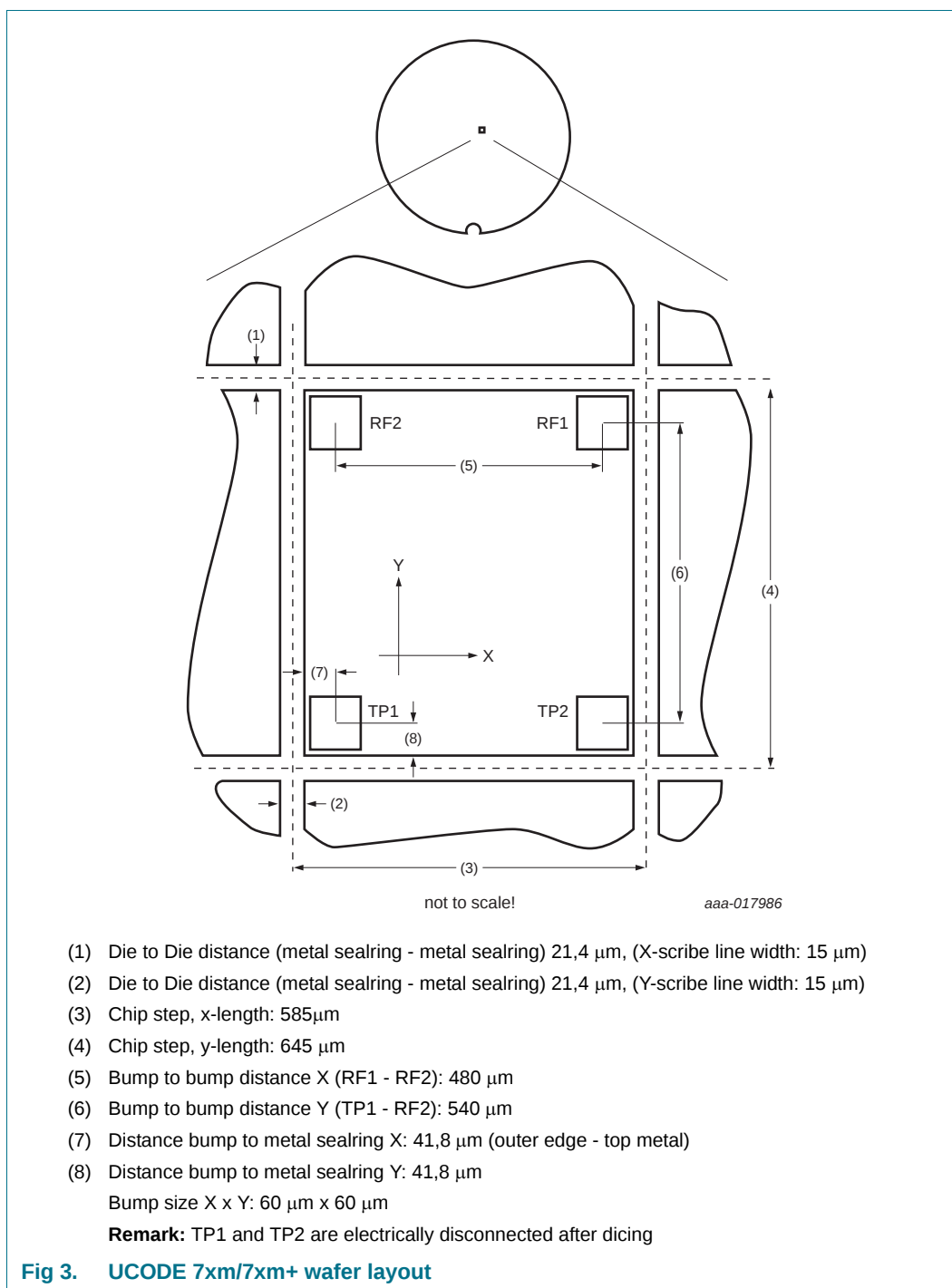
6.1 Pin description

Table 2. Pin description bare die

Symbol	Description
TP1	test pad 1
RF1	antenna connector 1
TP2	test pad 2
RF2	antenna connector 2

7. Wafer layout

7.1 Wafer layout



8. Mechanical specification

The UCODE 7xm/7xm+ wafers are available in 120 μm thickness with 7 μm Polyimide spacer, resulting in less coupling between the antenna and the active circuit.

8.1 Wafer specification

See [Ref. 4 "Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093**"](#).

8.1.1 Wafer

Table 3. Specifications

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	200 mm (8") unsawn - 205 mm typical sawn on foil
Thickness	120 $\mu\text{m} \pm 15 \mu\text{m}$
Number of pads	4
Pad location	non diagonal / placed in chip corners
Distance pad to pad RF1-RF2	480.0 μm
Distance pad to pad TP1-RF2	540.0 μm
Process	CMOS 0.14 μm
Batch size	25 wafers
Potential good dies per wafer	77.773
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 μm , R_t max. 5 μm
Chip dimensions	
Die size excluding scribe	0.570 mm $\times$ 0.630 mm = 0.359 mm ²
Scribe line width:	x-dimension = 15 μm
	y-dimension = 15 μm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 μm total thickness of passivation
Polyimide spacer	7 $\mu\text{m} \pm 1 \mu\text{m}$
Au bump	
Bump material	> 99.9 % pure Au
Bump hardness	35 – 80 HV 0.005
Bump shear strength	> 70 MPa
Bump height	25 μm ^[1]
Bump height uniformity	

Table 3. Specifications

within a die	$\pm 2 \mu\text{m}$
– within a wafer	$\pm 3 \mu\text{m}$
– wafer to wafer	$\pm 4 \mu\text{m}$
Bump flatness	$\pm 1.5 \mu\text{m}$
Bump size	
– RF1, RF2	$60 \times 60 \mu\text{m}$
– TP1, TP2	$60 \times 60 \mu\text{m}$
Bump size variation	$\pm 5 \mu\text{m}$

[1] Because of the $7 \mu\text{m}$ spacer, the bump will measure $18 \mu\text{m}$ relative height protruding the spacer.

8.1.2 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See [Ref. 4 “Data sheet - Delivery type description – General specification for 8” wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093**”](#)

8.1.3 Map file distribution

See [Ref. 4 “Data sheet - Delivery type description – General specification for 8” wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093**”](#)

9. Functional description

9.1 Air interface standards

The UCODE 7xm/7xm+ fully supports all mandatory parts of the EPCglobal v1.2.0 specification.

9.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE 7xm/7xm+ IC. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum possible power for the UCODE 7xm/7xm+ on the tag.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a rectified DC voltage to the analog and digital modules of the IC.

The antenna attached to the chip may use a DC connection between the two antenna pads. Therefore the UCODE 7xm/7xm+ also enables loop antenna design.

9.3 Data transfer

9.3.1 Interrogator to tag Link

An interrogator transmits information to the UCODE 7xm/7xm+ by modulating a UHF RF signal. The UCODE 7xm/7xm+ receives both information and operating energy from this RF signal. Tags are passive, meaning that they have no battery and receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. It communicates to the UCODE 7xm/7xm+ by modulating an RF carrier.

For further details refer to [Ref. 1](#).

9.3.2 Tag to interrogator Link

Upon transmitting a valid command an interrogator receives information from a UCODE 7xm/7xm+ tag by transmitting an un-modulated RF carrier and listening for a backscattered reply. The UCODE 7xm/7xm+ backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent. For further details refer to [Ref. 1](#).

9.4 UCODE 7xm and UCODE 7xm+ Overview

This table should provide a quick overview on the features implemented in UCODE 7xm and UCODE 7xm+. Details on the features are described in the following paragraphs.

Table 4. Overview of UCODE 7xm and UCODE 7xm+

Features	UCODE 7xm	UCODE 7xm+
User Memory	1024 bit	2048 bit
EPC Memory	max 448 bit	max 448 bit
TID Memory	96 bit	96 bit
Access Password	32 bit	32 bit
Kill Password	32 bit	32 bit
PSF (Product Status Flag)	yes	yes
BlockWrite (32 bit)	yes	yes
BlockPermalock (256 bit block size)	yes	yes
Pre-Serialization of 96-bit EPC	yes	yes
Parallel Encoding	yes	yes
Backscatter strength reduction	yes	yes
Tag Power Indicator	yes	yes
Untraceable feature	yes	yes
Digital Signature (384-bit)	-	yes

9.5 Supported commands

The UCODE 7xm/7xm+ support all **mandatory** EPCglobal v1.2.0 commands.

In addition the following **optional** commands are supported:

- Access
- BlockPermalock (256 bit block size)
- BlockWrite (max 32 bit on even addresses only)

UCODE 7xm/7xm+ also offers the following **custom** commands:

- Untraceable
- ReadSignature (UCODE 7xm+ only)

9.5.1 Custom commands

9.5.1.1 Untraceable

The Untraceable function allows the UCODE 7xm/7xm+ to hide the complete or parts of the EPC, TID and/or user memory. In addition the read range can be completely or temporarily reduced.

This command can only be executed from the secured state.

Memory parts which are set untraceable are acting as non-existing.

EPC-field:

Specifies the number of words of the EPC memory which the UCODE 7xm/xm+ backscatters. A change of this field therefore also changes the L bit in the Protocol Control (PC) word.

TID-field:

Hide some ("01") will hide the TID memory from address 20h (included) onwards.

Range-field:

In case of activated range toggling the read range reduction toggles from the actual value to the second. (e.g. when actual state is normal it toggles to reduced). In case of power loss the chip reverts to it's prior state

UCODE 7xm/7xm+ does not support the U bit and therefore ignores this value.

Table 5. Untraceable command

	Command	RFU	U	EPC	TID	User	Range	RN	CRC
No. of bits	16	2	1	6	2	1	2	16	16
Description	1110 0010 0000 0000	00	don't care	MSB: "0": show memory above EPC "1": hide memory above EPC 5 LSBs: New EPC length	"00": hide none "01": hide some "10": hide all "11": RFU	"0": view "1": hide	"00": normal "01": toggle "10": reduced "11": RFU	handle	CRC-16

Table 6. Untraceable command-response table

Starting State	Condition	Response	Next State
ready	all	-	ready
arbitrate, reply, acknowledged	all	-	arbitrate
open	all	-	open
secured	executable	backscatter header when done	secured
killed	all	-	killed

In case of an access to the tag the error condition "memory overrun" will be returned.

9.5.1.2 ReadSignature (UCODE 7xm+ only)

The ReadSignature command allows the read out of the pre-programmed Digital Signature and includes a CRC-16 calculated over the whole command, the handle and the a frame-sync.

Table 7. ReadSignature command

	Command	WordPtr	WordCount	RN	CRC
No. of bits	16	EVB	8	16	16
Description	1110 0000 0000 1000	Starting Address Pointer	Number of words to read	Handle	CRC-16

Table 8. Tag reply to a successful ReadSignature command

	Header	Signature Words	RN	CRC
No. of bits	1	Variable	16	16
Description	0	Digital Signature	Handle	CRC-16

The error Response “memory overrun” is returned in case WordCount=0 or in case WordPtr or the combination of WordPtr and WordCount exceeds the range of the Digital Signature.

Table 9. ReadSignature command-response table

Starting State	Condition	Response	Next State
ready	all	-	ready
arbitrate, reply, acknowledged	all	-	arbitrate
open	all	backscatter data	open
secured	all	backscatter data	secured
killed	all	-	killed

Digital Signature

The UCODE 7xm+ is delivered with a factory pre-programmed 384-bit Digital Signature based on the Elliptic Curve Digital Signature Algorithm (ECDSA) using a 192-bit cryptographic key. The parameters of the curve are according NIST P-192 (secp 192r1). The data digital signed is the 96-bit TID of the UCODE 7xm+.

Verification of the digital signature:

After issuing the ReadSignature command the tag will return the 384-bit digital signature. With the knowledge of the Public Key and the algorithm a verification that the silicon is an origin NXP Semiconductors can be made.

UCODE 7xm+ Public Key:

04A72DB4B83233DD9A9711DB071281F14451747F815EEB111F1D4CD3DCAD60250C
830CD287DCEC0B39C76262BA998B7E01

MS VC++ Code Example

```

/**
 * Check Originality Signature on curve NID_X9_62_prime192v1
 **/

unsigned char CheckOriginalitySignature192UCODE7xmBinary(unsigned char * aUId,
unsigned char * aSignature)

{
    /* secp192v1 => ECC_Length=24; */
    unsigned int ECC_Length = 24;
    unsigned int bLength = 12;
    char* publickey_str =
    "04A72DB4B83233DD9A9711DB071281F14451747F815EEB111F1D4
    CD3DCAD60250C830CD287DCEC0B39C76262BA998B7E01"; /* UCODE7xm */

    BIGNUM *pk_bignum = BN_new();
    EC_POINT *public_key = NULL;

    /* Create a EC_KEY for specified curve */

    EC_KEY *pubKey = EC_KEY_new_by_curve_name(NID_X9_62_prime192v1);
    const EC_GROUP *ecgroup = EC_KEY_get0_group(pubKey);
    ECDSA_SIG *signature = ECDSA_SIG_new();
    unsigned char r[24]; /* ECC_Length */
    unsigned char s[24]; /* ECC_Length */
    char r_dest[24*2+1]; /* ECC_Length *2 +1 */
    char s_dest[24*2+1]; /* ECC_Length *2 +1 */
    unsigned int loop = 0;
    if (signature == NULL )
    {
        return 1;
    }
    if (pubKey == NULL)
    {
        printf("Creation of PubKey failed \n");
        return 1;
    }

    /* Convert the hex public key x,y co-ordinates to BIGNUM */

    BN_hex2bn(&pk_bignum, publickey_str);
    public_key = EC_POINT_bn2point(ecgroup, pk_bignum, NULL, NULL);

    /* Set the public key point to EC_KEY */

    EC_KEY_set_public_key(pubKey, public_key);

```

```
/* Extract the r and s part of the signature*/

memcpy(r, aSignature, ECC_Length);
memcpy(s, aSignature+ECC_Length, ECC_Length);

/* BIGNUM conversion function expects r in ASCII value */

for(loop = 0; loop < ECC_Length; loop++)
{
    sprintf_s((r_dest+(loop*2)), 3, "%02X", r[loop]);
    sprintf_s((s_dest+(loop*2)), 3, "%02X", s[loop]);
}

BN_hex2bn(&signature->r, r_dest);
BN_hex2bn(&signature->s, s_dest);

/*Signature verification for the UID sent*/

if (ECDSA_do_verify(aUid, bLength, signature, pubKey) == 1)
{
    printf("\nSignature verified successfully\n\n");
    return 0;
}
else
{
    printf("\nSignature verification failed\n\n");
    return 1;
}
}
```

9.6 UCODE 7xm/7xm+ memory

The UCODE 7xm/7xm+ memory is implemented according EPCglobal v1.2.0 and organized in four banks:

Table 10. UCODE 7xm memory sections

Name	Size	Bank
Reserved memory (32 bit ACCESS and 32 bit KILL password)	64 bit	00b
EPC (excluding CRC, PC)	448 bit	01b
TID (including permalocked unique 48 bit serial number)	96 bit	10b
User Memory	1024bit	11b

Table 11. UCODE 7xm+ memory sections

Name	Size	Bank
Reserved memory (32 bit ACCESS and 32 bit KILL password)	64 bit	00b
EPC (excluding CRC, PC)	448 bit	01b
TID (including permalocked unique 48 bit serial number)	96 bit	10b
User Memory	2048bit	11b

The logical address of all memory banks begin at zero (00h).

In addition to the four memory banks a **configuration word** to handle the UCODE 7xm/7xm+ specific features is available at address 200h in the EPC memory. The configuration word is described in detail in [Section 9.7.1 "UCODE 7xm/7xm+ features control mechanism"](#).

The TID complies to the extended tag Identification scheme according GS1 EPC Tag Data Standard 1.9. ([Ref. 2](#))

9.6.1 UCODE 7xm/7xm+ overall memory map

Table 12. UCODE 7xm/7xm+ overall memory map

Bank address	Memory address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	1b	locked memory
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 1DFh	EPC	EPC	[1]	unlocked memory
Bank 01 ConfigWord	200h	EPC	RFU	0b	locked memory
	201h	EPC	RFU	0b	locked memory
	202h	EPC	Parallel encoding	0b	Action bit[4]
	203h	EPC	RFU	0b	locked memory
	204h	EPC	Tag Power Indicator	0b	Action bit[4]
	205h	EPC	RFU	0b	locked memory
	206h	EPC	RFU	0b	locked memory
	207h	EPC	RFU	0b	locked memory
	208h	EPC	RFU	0b	locked memory
	209h	EPC	max. backscatter strength	1b	permanent bit[5]
	20Ah	EPC	RFU	0b	locked memory
	20Bh	EPC	RFU	0b	locked memory
	20Ch	EPC	RFU	0b	locked memory
	20Dh	EPC	RFU	0b	locked memory
	20Eh	EPC	RFU	0b	locked memory
	20Fh	EPC	PSF alarm flag	0b	Permanent bit[5]
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	806h	locked memory
	14h	TID	config word indicator	1b[2]	locked memory
	14h to 1Fh	TID	tag model number	TMNR[3]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory
Bank 11 USER	000h to 3FFh	USER	User Memory	undefined	locked memory UCODE 7xm and 7xm+
	400h to 7FFh	USER	User Memory	undefined	locked memory UCODE 7xm+ only

[1] HEX E280 6000 0000 nnnn nnnn nnnn
where n are the nibbles of the 48-bit SNR of the TID

[2] Indicates the existence of a Configuration Word at the end of the EPC number

[3] See [Figure 4](#)

- [4] Action bits: meant to trigger a feature upon a SELECT command on the related bit ref feature control mechanism, see [Section 9.7.1](#)
- [5] Permanent bit: permanently stored bits in the memory; Read/Writeable according to EPC bank lock status, see [Section 9.7.1](#)

9.6.2 UCODE 7xm/7xm+ TID memory details

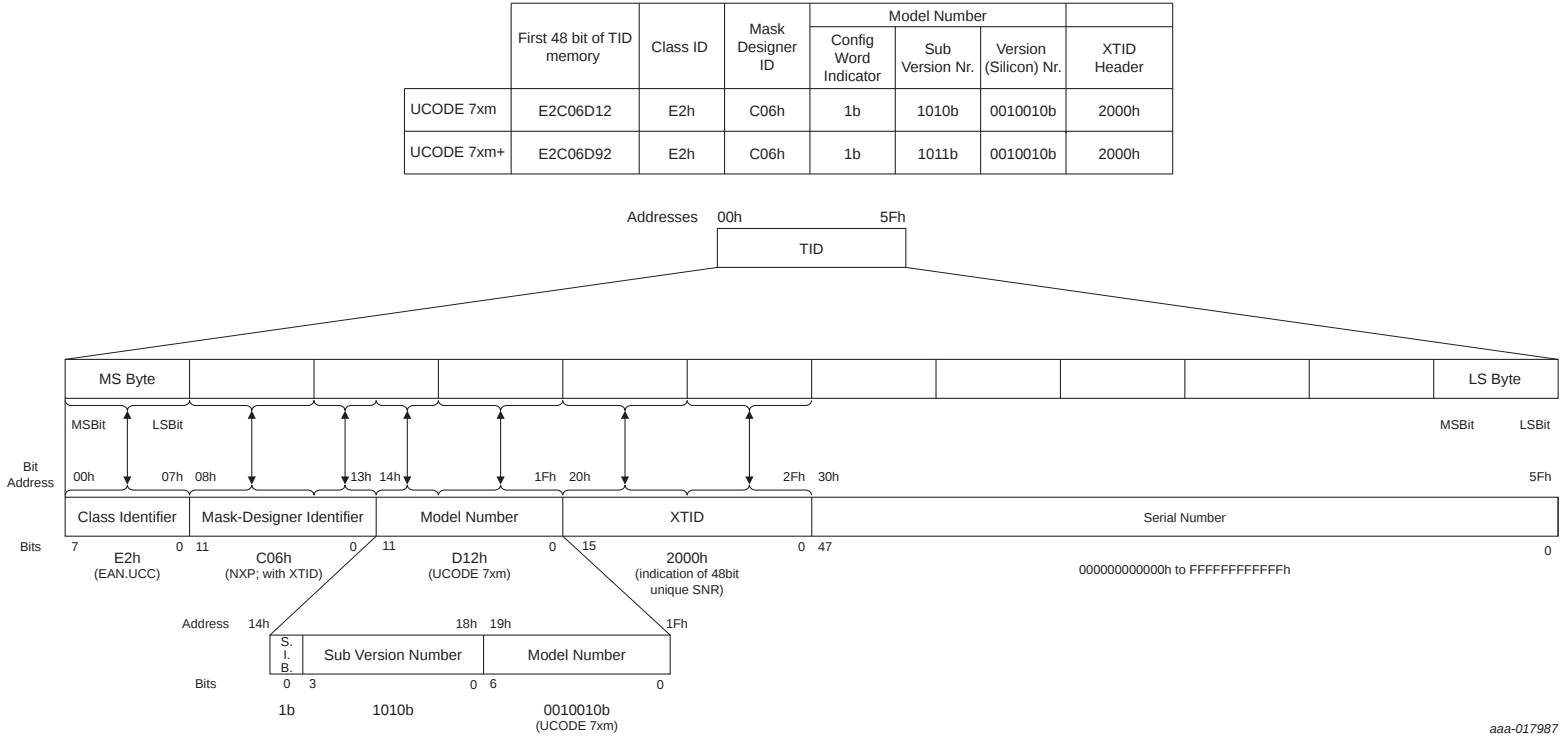


Fig 4. UCODE 7xm/7xm+ TID memory structure

9.7 Supported features

The UCODE 7xm/7xm+ is equipped with features of previous UCODE generation. These include:

- Pre-serialization of the 96-bit EPC
- Parallel encoding
- Tag Power Indicator
- Backscatter strength reduction
- Product Status Flag (PSF)
- Single-slit antenna solution

These features are implemented in such a way that standard EPCglobal v1.2.0 READ / WRITE / ACCESS / SELECT commands can be used to operate these features.

The Configuration Word, as mentioned in the memory map, describes the additional features located at address 200h of the EPC memory.

Bit 14h of the TID indicates the existence of a Configuration Word. This flag will enable the selection of configuration word enhanced transponders in mixed tag populations.

9.7.1 UCODE 7xm/7xm+ features control mechanism

The different features of the UCODE 7xm/7xm+ can be activated / de-activated by addressing or changing the content of the corresponding bit in the configuration word located at address 200h in the EPC memory bank (see [Table 13](#)). The de-activation of the action bit features will only happen after chip reset.

Table 13. Configuration word UCODE 7xm/7xm+

Locked memory		Action bit	Locked memory	Action bit	Locked memory		
RFU	RFU	Parallel encoding	RFU	Tag Power Indicator	RFU	RFU	RFU
0	1	2	3	4	5	6	7

Table 14. Configuration word UCODE 7xm/7xm+

Locked memory	Permanent bit	Locked memory					Permanent bit
RFU	max. backscatter strength	RFU	RFU	RFU	RFU	RFU	PSF Alarm bit
8	9	10	11	12	13	14	15

The configuration word contains 2 different type of bits:

- **Action bits:** meant to trigger a feature upon a SELECT command on the related bit:
Parallel encoding
Tag Power indicator

- **Permanent bits:** permanently stored bits in the memory

Max. Backscatter Strength

PSF Alarm bit

The activation or the de-activation of the feature behind the permanent bits happens only when attempting to write a "1" value to the related bit (value toggling) - writing "0" value will have no effect.

If the feature is activated, the related bit will be read with a "1" value and, if de-activated, with a "0" value.

The permanent bits can only be toggled by using standard EPC WRITE (not a BlockWrite) if the EPC bank is unlocked or within the SECURED state if the EPC is locked. If the EPC is permalocked, they cannot be changed.

Action bits will trigger a certain action only if the pointer of the SELECT command exactly matches the action-bit address (i.e. 202h or 204h), if the length=1 and if mask=1b (no multiple trigger of actions possible within one single SELECT command).

After issuing a SELECT to any action bits an interrogator shall transmit CW for RTCal [Ref. 3](#) + 80 µs before sending the next command.

If the truncate bit in the SELECT command is set to "1" the SELECT will be ignored.

A SELECT on action bits will not change the digital state of the chip.

The action bits can be triggered regardless if the EPC memory is unlocked, locked or permalocked.

9.7.2 Backscatter strength reduction

The UCODE 7xm/7xm+ features two levels of backscatter strengths. Per default maximum backscatter is enabled in order to enable maximum read rates. When clearing the flag the strength can be reduced if needed.

9.7.3 Automatic self pre-serialization of the 96-bit EPC

Description

The 96-bit EPC, which is the initial EPC length settings of UCODE 7xm/7xm+, will be delivered pre-serialized with the 48-bit serial number from the TID.

Use cases and benefits

With a pre-serialized EPC, the encoding process of the tags with UCODE 7xm/7xm+ gets simpler and faster as it only needs to encode the SKU (58-bit header of the EPC).

9.7.4 Parallel encoding

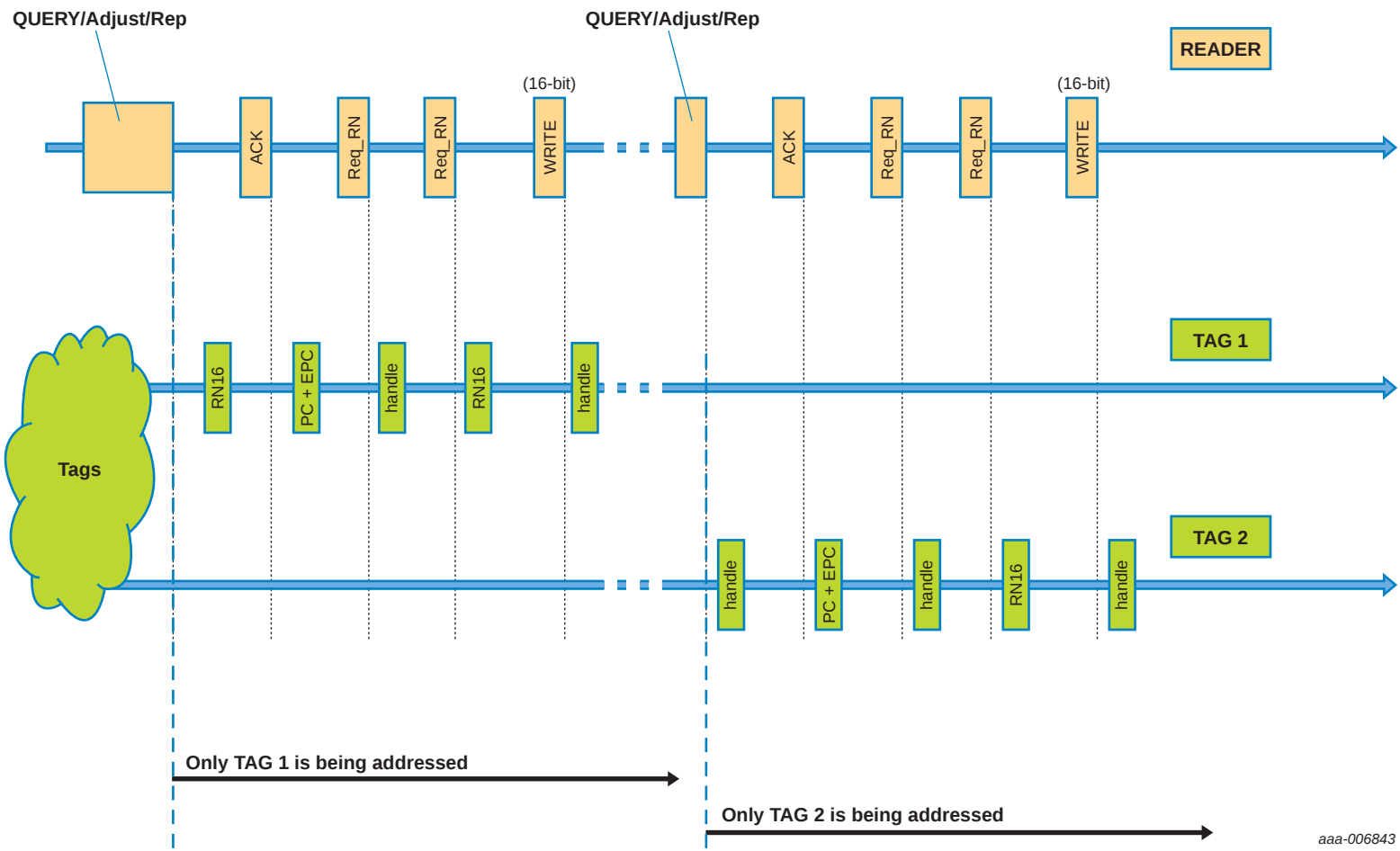
Description

This feature of the UCODE 7xm/7xm+ can be activated by the “Parallel encoding bit” in the Configuration-Word located at (202h).

Upon issuing a EPC SELECT command on the “Parallel encoding bit”, in a population of UCODE 7xm/7xm+ tags, a subsequent QUERY brings all tags go the OPEN state with a specific handle (“AAAAh”).

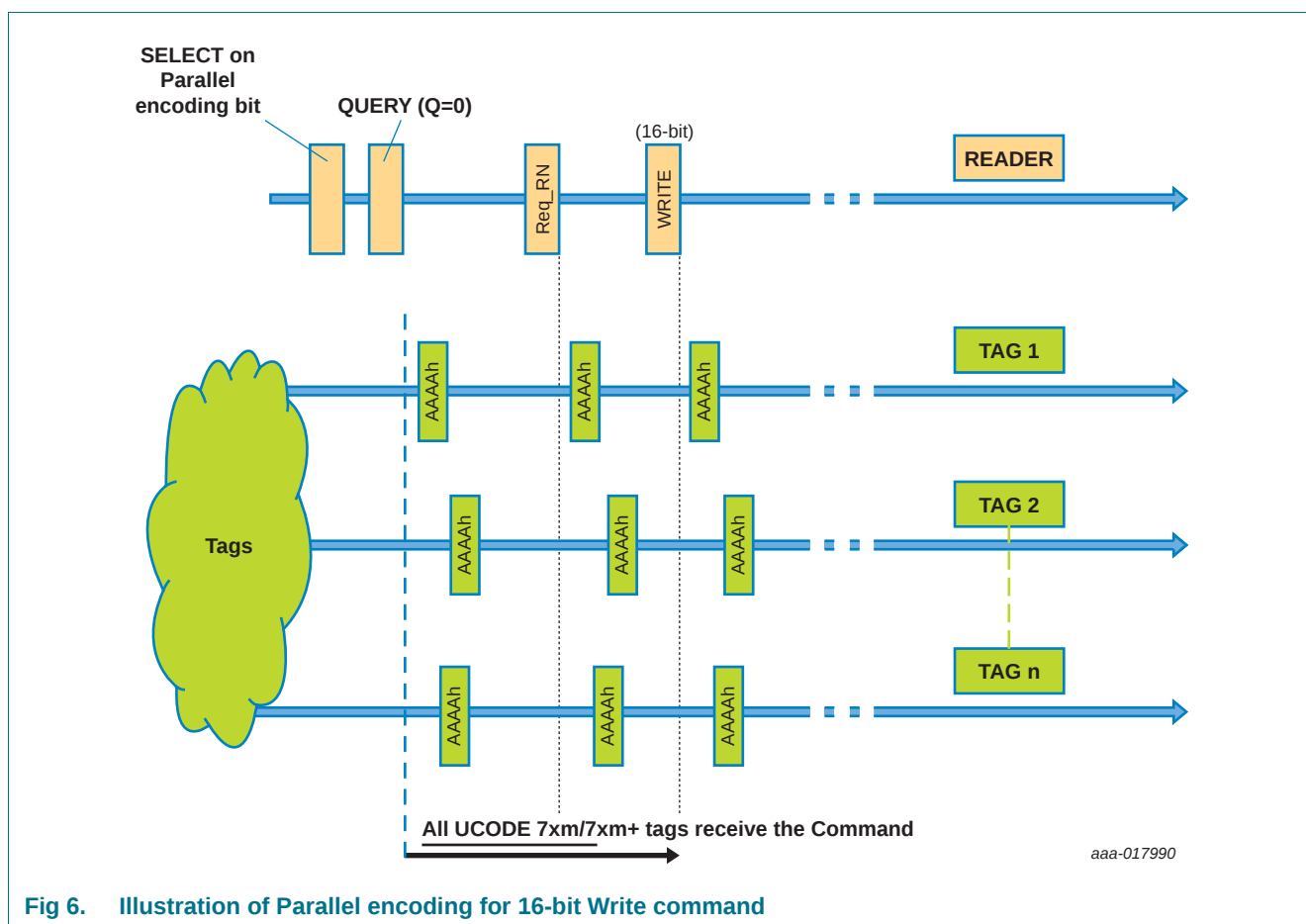
Once in the OPEN state, for example a WRITE command will apply to all tags in the OPEN state (see [Figure 6](#)). This parallel encoding is considerably lowering the encoding time compared to a standard implementation (see [Figure 5](#)).

The amount of tags that can be encoded at the same time will depend on the strength of the reader signal. Since all tags will backscatter their ACKNOWLEDGE (ACK) response at the same time, the reader will observe collision in the signal from the tags.



aaa-006843

Fig 5. Example of 16-bit Write command with standard EPC Gen 2 commands



Use cases and benefits

Parallel encoding feature of UCODE 7xm/7xm+ can enable ultra fast bulk encoding.

Taking in addition advantage of the pre-serialization scheme of UCODE 7xm/7xm+, the same SKU can be encoded in multiple tags as the EPC will be delivered pre-serialized already.

In the case of only one tag answering (like in printer encoding), this feature could be used to save some overhead in commands to do direct EPC encoding after the handle reply.

Since this is a custom specific feature of UCODE 7xm/7xm+ (taken over from our previous UHF tag IC UCODE 7/7m) the use of this features requires the same support on the reader side as for previous UCODE products.

9.7.5 Tag Power Indicator

Description

Upon a SELECT command on the “Tag Power Indicator”, located in the config word 204h, an internal power check on the chip is performed to see if the power level is sufficient to perform a WRITE command. The decision level is defined as nominal WRITE sensitivity minus 1dB. In the case there is enough power, the SELECT command is matching and non-matching if not enough power. The tag can then be singulated by the standard inventory procedure.

Use cases and benefits

This feature gives the possibility to select only the tag(s) that receive enough power to be written during e.g. printer encoding in a dense environment of tags even though the reader may read more than one tag (see [Figure 7](#) for illustration). The power level still needs to be adjusted to transmit enough writing power to one tag only to do one tag singulation.

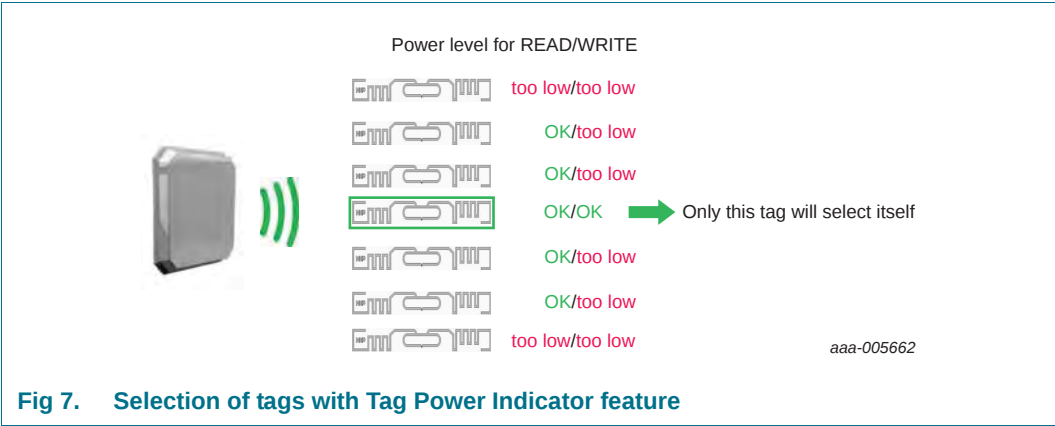


Fig 7. Selection of tags with Tag Power Indicator feature

9.7.6 Product Status Flag (PSF)

Description

The PSF is a general purpose bit located in the Configuration word at address 20Fh with a value that can be freely changed.

Use cases and benefits

The PSF bit can be used as an EAS (Electronic Article Surveillance) flag, quality checked flag or similar.

In order to detect the tag with the PSF activated, a EPC SELECT command selecting the PSF flag of the Configuration word can be used. In the following inventory round only PSF enabled chips will reply their EPC number.

9.7.7 Single-slit antenna solution

Description

In UCODE 7xm/7xm+ the test pads TP1 and TP2 are electrically disconnected meaning they are not electrically active and can be safely short-circuited to the RF pads RF1 and RF2 (see [Figure 8](#)).

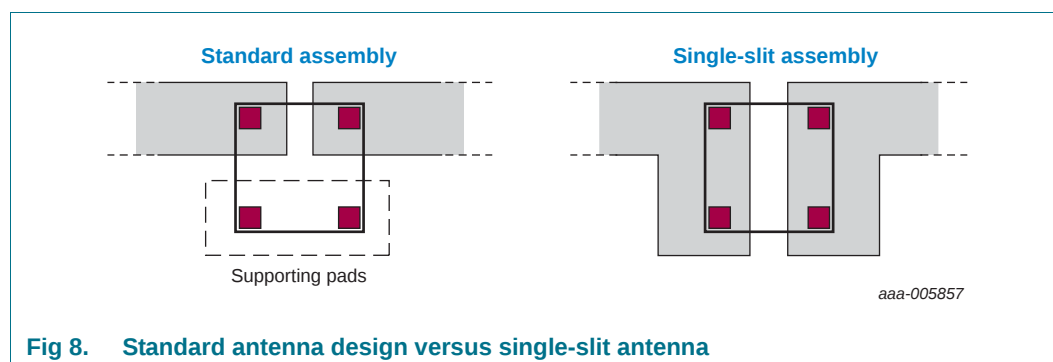


Fig 8. Standard antenna design versus single-slit antenna

Uses cases and benefits

Using single-slit antenna enables easier assembly and antenna design. Inlay manufacturer will only have to take care about one slit of the antenna instead of two in case all pads need to be disconnected from each other.

Additionally single-slit antenna assembly and the related increased input capacitance (see [Table 16](#)) can be used advantageously over the standard antenna design as additional room for optimization to different antenna design.

10. Limiting values

Table 15. Limiting values^{[1][2]}

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages are referenced to RFN

Symbol	Parameter	Conditions		Min	Max	Unit
Bare die limitations						
T _{stg}	storage temperature			–55	+125	°C
T _{amb}	ambient temperature			–40	+85	°C
V _{ESD}	electrostatic discharge voltage	Human body model	^[3]	-	± 2	kV
Pad limitations						
P _i	input power	maximum power dissipation, RFP pad		-	100	mW

- [1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.
- [2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- [3] For ESD measurement, the die chip has been mounted into a CDIP20 package.

11. Characteristics

11.1 UCODE 7xm/7xm+ bare die characteristics

Table 16. UCODE 7xm/7xm+ RF interface characteristics (RF1, RF2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			840	-	960	MHz
$P_{i(min)}$	minimum input power	READ sensitivity	[1][3][8]	-	-18.5	-	dBm
$P_{i(min)}$	minimum input power	WRITE sensitivity	[2]	-	-12	-	dBm
$P_{i(min)}$	minimum input power	Reduced operating range	[2]	-	+7	-	dBm
t	encoding speed (16b-bit or 32-bit)	16-bit	[5]	-	1.5	-	ms
C_i	chip input capacitance	parallel	[3][4]	-	0.63	-	pF
Z	chip impedance	866 MHz	[3][4]	-	19-j284	-	Ω
		915 MHz	[3][4]	-	17-j274	-	Ω
		953 MHz	[3][4]	-	17-j265	-	Ω
Z	typical assembled impedance [9]	915 MHz	[6]	-	26-j235	-	Ω
Z	typical assembled impedance [9] in case of single-slit antenna assembly	915 MHz	[6][7]	-	16-j181	-	Ω
Tag Power Indicator mode							
$P_{i(min)}$	minimum input power level to be able to select the tag		[2]	-	-11	-	dBm

[1] Power to process a QUERY command

[2] Tag sensitivity on a 2dBi gain antenna

[3] Measured with a 50 Ω source impedance directly on the chip

[4] At minimum operating power

[5] When the memory content is "0000...".

[6] The antenna shall be matched to this impedance

[7] Depending on the specific assembly process, sensitivity losses of few tenths of dB might occur

[8] Results in approximately -19dBm tag sensitivity with a 2dBi gain antenna

[9] Assuming a 80fF additional input capacitance, 250fF in case of single slit antenna

Table 17. UCODE 7xm/7xm+ memory characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
EEPROM characteristics							
t_{ret}	retention time	$T_{amb} \leq 55\text{ }^{\circ}\text{C}$		20	-	-	year
$N_{endu(W)}$	write endurance			100k	-	-	cycle

12. Package outline

This section is not applicable for this kind of device.

13. Packing information

13.1 Wafer

See [Ref. 4 "Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093**"](#)

14. Abbreviations

Table 18. Abbreviations

Acronym	Description
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DSB-ASK	Double Side Band-Amplitude Shift Keying
DC	Direct Current
EAS	Electronic Article Surveillance
EEPROM	Electrically Erasable Programmable Read Only Memory
EPC	Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number)
FM0	Bi phase space modulation
G2	Generation 2
IC	Integrated Circuit
PIE	Pulse Interval Encoding
PSF	Product Status Flag
RF	Radio Frequency
UHF	Ultra High Frequency
SECS	Semi Equipment Communication Standard
TID	Tag Identifier

15. References

- [1] GS1 EPCglobal: EPC™ Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.2.0 (23 October 2008)
- [2] EPCglobal: EPC Tag Data Standard Version 1.9, ratified Nov-2014
- [3] RTCal is the Interrogator-to-Tag calibration symbol length defined in the EPCglobal specification
- [4] Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093**¹

1. ** ... document version number

16. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SL3S1004_1014 v.3.2	20160727	Product data sheet	-	SL3S1004_1014 v.3.1
Modifications:	• Update Automatic Pre-serialization functionality			
SL3S1004_1014 v.3.1	20150727	Product data sheet	-	SL3S1004_1014 v.3.0
Modifications:	• Update UCODE 7xm+ Public Key			
SL3S1004_1014 v.3.0	20150615	Product data sheet	-	SL3S1004_1014 v.1.0
Modifications:	• Update Write sensitivity • Digital Signature explanation and source code added • Update of final feature set • Editorial changes			
SL3S1004_1014 v.1.0	20150416	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b)

whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

UCODE — is a trademark of NXP B.V.

18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

19. Contents

1	General description	1	9.7.4	Parallel encoding	21
2	Features and benefits	1		Description	21
2.1	Key features	1		Use cases and benefits	23
2.1.1	Memory	2	9.7.5	Tag Power Indicator	24
2.2	Key benefits	2		Description	24
2.2.1	End user benefit	2		Use cases and benefits	24
2.2.2	Antenna design benefits	2	9.7.6	Product Status Flag (PSF)	25
2.2.3	Label/module manufacturer benefit	2		Description	25
2.3	Supported features	2		Use cases and benefits	25
3	Applications	3	9.7.7	Single-slit antenna solution	25
3.1	Markets	3		Description	25
3.2	Applications	3		Uses cases and benefits	25
4	Ordering information	3	10	Limiting values	26
5	Block diagram	4	11	Characteristics	27
6	Pinning information	5	11.1	UCODE 7xm/7xm+ bare die characteristics	27
6.1	Pin description	5	12	Package outline	28
7	Wafer layout	6	13	Packing information	28
7.1	Wafer layout	6	13.1	Wafer	28
8	Mechanical specification	7	14	Abbreviations	28
8.1	Wafer specification	7	15	References	29
8.1.1	Wafer	7	16	Revision history	30
8.1.2	Fail die identification	8	17	Legal information	31
8.1.3	Map file distribution	8	17.1	Data sheet status	31
9	Functional description	9	17.2	Definitions	31
9.1	Air interface standards	9	17.3	Disclaimers	31
9.2	Power transfer	9	17.4	Trademarks	32
9.3	Data transfer	9	18	Contact information	32
9.3.1	Interrogator to tag Link	9	19	Contents	33
9.3.2	Tag to interrogator Link	9			
9.4	UCODE 7xm and UCODE 7xm+ Overview	10			
9.5	Supported commands	10			
9.5.1	Custom commands	11			
9.5.1.1	Untraceable	11			
9.5.1.2	ReadSignature (UCODE 7xm+ only)	12			
	Digital Signature	12			
9.6	UCODE 7xm/7xm+ memory	15			
9.6.1	UCODE 7xm/7xm+ overall memory map	16			
9.6.2	UCODE 7xm/7xm+ TID memory details	18			
9.7	Supported features	19			
9.7.1	UCODE 7xm/7xm+ features control mechanism	19			
9.7.2	Backscatter strength reduction	20			
9.7.3	Automatic self pre-serialization of the 96-bit EPC	20			
	Description	20			
	Use cases and benefits	20			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 July 2016
325032